APPARATUS AND METHOD FOR LEAKAGE COMPENSATION IN THIN OXIDE CMOS APPLICATIONS

TECHNICAL FIELD

The present invention relates generally to the field of Complementary Metal-Oxide Semiconductor (CMOS) technology and, more particularly, to ameliorating device current leakage.

BACKGROUND

The progress of electronic circuits was accomplished partially, as a result of the downsizing of components, such as vacuum tubes, for more than a century. The downsizing of active or passive components decreases their capacitance, resulting in an increase of the circuit operating speed and decrease of its power consumption. The size reduction increases the component density in the circuit, and enhances parallel operation capability, resulting in another increase in the circuit speed.

Historically, Field Effect Transistor (FET) technology scaling trends seek to improve gate delay by about 30% and the reduction of transition-energy by approximately 30% to 65% per generation. Typically, this is accomplished by scaling supply voltages and/or shrinking the process technology. In developing semiconductors, maximum supply

voltages are limited by gate oxide wear-out, and minimum supply voltage levels are typically set by practical noise-margin and performance considerations. The components, though, should maintain proper device behavior at smaller and smaller channel lengths and progressively thinner gate dielectrics, which is in turn dependent on maintaining an adequately large lateral-to-vertical aspect ratio for a device. Thus, the ability to scale semiconductor gate dielectrics can be limited by both the scalability of the supply voltage and the desire to preserve the device's aspect ratio.

Static Random Access Memory (SRAM) circuits, for example in sub-0.3μm CMOS technologies, exhibit profound read sensitivities to increased leakage current. Due to the limited scalability in supply voltages in high-performance applications, high electric fields may develop across the thin (~1.5nm) Silicon Dioxide (SiO_2) gate oxide. This field distorts the silicon band gap, such that electrons may more easily travel from the valence to the conduction band, from the gate to the channel and body. This problem is known as tunneling. This tunneling current along with sub-threshold leakage mechanisms, combine to affect the buildup of a voltage differential between the SRAM's bit lines such that the current-sinking behavior of the selected SRAM cell's wordline means Negative-Channel FETs (NFETs) must contend

with significant leakage current from the non-selected devices.

It can be difficult to predict the limit of the down-sizing, although the ultimate limit of the downsizing is the distance of atoms in silicon crystals and that is about 0.3 nm. Some signal moderation effect such as through a single atomic size gate electrode might be possible, but the moderated signal would be too weak to transfer to another node. In addition, there is no practical solution at this moment for interconnects to contact to such small atomic nodes. Thus, the limit of the downsizing is considered from the viewpoint of the integration of individual components into circuits.

Therefore, there is a need for a device that addresses at least some of the issues related to integration limits, performance limits, power increases, reliability factors and design/production costs until integrated devices development expands beyond CMOS type devices.

SUMMARY OF THE INVENTION

The present invention provides a method for current leakage correction for a leaky capacitor. A voltage across the leaky capacitor is measured. The measured voltage to a scaled capacitor is provided, wherein the scaled capacitor has an area reduced by a scaling factor in comparison to the

leaky capacitor. Also, a sustaining charge to the leaky capacitor is provided.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following Detailed Description taken in conjunction with the accompanying drawings, in which:

FIGURE 1A is a block diagram depicting a circuit containing a thin oxide leaky capacitor;

FIGURE 1B is a graph depicting an ideal voltage across a capacitor relative to a current pulse;

FIGURE 2 is a timing diagram of Phased Lock Loop (PLL) filter capacitor voltage affected by a leakage current resulting in a static phase error; and

FIGURE 3 is a block diagram depicting a leakage correction circuit coupled to a thin oxide leaky capacitor.

DETAILED DESCRIPTION

In the following discussion, numerous specific details are set forth to provide a thorough understanding of the present invention. However, those skilled in the art will appreciate that the present invention may be practiced without such specific details. In other instances, well-known elements have been illustrated in schematic or block

diagram form in order not to obscure the present invention in unnecessary detail. Additionally, for the most part, details concerning network communications, electro-magnetic signaling techniques, and the like, have been omitted inasmuch as such details are not considered necessary to obtain a complete understanding of the present invention, and are considered to be within the understanding of persons of ordinary skill in the relevant art.

It is further noted that, unless indicated otherwise, all functions described herein may be performed in either hardware or software, or some combination thereof. In one embodiment, however, the functions can be performed by a processor, such as a computer or an electronic data processor, in accordance with code, such as computer program code, software, and/or integrated circuits that are coded to perform such functions, unless indicated otherwise. In the present specification, the same reference characters are used to refer to terminals, signal lines, and their corresponding signals.

Referring to FIGURES 1A and 1B of the drawings, the reference numeral 100 generally designates a block diagram depicting a circuit containing a thin oxide leaky capacitor. Also, the reference numeral 150 generally designates is a graph depicting an ideal voltage across a capacitor relative to a current pulse. The circuit 100 comprises a current

source 102, a capacitor 104, a first leakage current source 106, and ground 108.

The circuit 100 is utilized in a variety of applications, such as PLLs. However, as a result of the thin film dielectric in the capacitor 104, leakage current across the capacitor 104 can substantially affect the behavior of the capacitor. The intention in the circuit 100 is to generate a voltage V_c of FIGURE 1B across the capacitor 104 of FIGURE 1A that is proportional to the width of a current pulse Δt of FIG. 1B.

If a high impedance path (not shown) is provided at the first node 110 between the current source 102 and the capacitor 104, then for hold states when the impedance is high, the voltage V_c of FIGURE 1B across the capacitor 104 of FIGURE 1A decreases due to leakage. In other words, when the current source 104 is effectively "shut off," the V_c of FIGURE 1B across the capacitor 104 of FIGURE 1A decreases at a rate higher than the normal rate of capacitive discharge. Thus, the voltage V_c of FIGURE 1B across the capacitor 104 of FIGURE 1A is as follows:

$$(1)\quad Vc = \frac{1}{C}\int Iup \cdot dt - \frac{1}{C}\int Ileak \cdot dt + Vc(0)$$

V_C is the output voltage across the capacitor. C is the electrical capacitance in Farads. I_{leak} is the leakage current in Amperes. I_{UP} is the height of the rise of current during the leading edge of a clock signal, and dt is the change in time (also known as D (delta time).

The circuit 100 operates by driving a current across a capacitor 104. A current source or charge pump 102 provides a current to a first node 110. Also, the current source 102 can be either a negative charge source or a positive charge source. A capacitor 104 is coupled to the first node 110 and to ground 108 at a second node 112. The charge leakage is represented by the first leakage current source 106. The first leakage current source 106 is coupled at first end to the first node 110 and at a second end to the second node 112.

Referring to FIGURE 2 of the drawings, the reference numeral 200 generally designates a timing diagram of PLL filter capacitor voltage affected by a leakage current resulting in a static phase error. In general, thin oxide capacitors do not have ideal electrical characteristics due to tunneling leakage.

Although the tunneling leakage is exponentially related to the voltage V_{C2} across a capacitor (not shown), FIGURE 2 is shown as a lineal representation. Also, I_{UP} and I_{PUMP} are the height of the rise of current during the leading edge of

a clock signal and a supply current, respectively. Since the capacitor voltage decreases due to leakage during the hold period of T minus T_{SPE}, a phase error T_{SPE} develops which the phase lock loop tries to correct at the next reference clock cycle, according to the following formula:

$$(2) \quad \int_{0}^{Tspe} Iup \cdot dt = \int_{Tspe}^{T} Ileak \cdot dt$$

This static phase error (SPE) results in a continuous phase error between the reference clock and the PLL feedback clock, causing tracking and cycle-cycle jitter, a potentially unstable loop and system failure.

Currently, several different methods are available to attempt to moderate or reduce the impact of SPE on a circuit. One method involves reducing leakage current across a capacitor (not shown) by reducing the capacitor area. However, this method can degrade loop performance since other loop parameters must be increased to compensate for a reduction in capacitance. Thicker oxides can be used, though these can introduce additional costs of manufacturing. Increasing a supply current I_{PUMP} may also result in difficulties maintaining optimal PLL characteristics. Lastly, adjustments to the reference clock

frequency, though these suffer from an effective minimum in present systems of $T \geq \sim 2$ nanoseconds.

Referring to FIGURE 3 of the drawings, the reference numeral 300 generally designates a block diagram depicting a leakage correction circuit coupled to a thin oxide leaky capacitor. The circuit 300 comprises a charge pump (CP) circuit 350 and a correction circuit 352. The CP 350 further comprises a current source 302, a first capacitor 304, ground 308, and a first leakage current source 306. The correction circuit 352 further comprises ground 308, a second capacitor 316, a second leakage current source 344, a first Positive-Channel Field Effect Transistor (PFET) 312, a second PFET 314, a first Negative-Channel Field Effect Transistor (NFET) 318, a second NFET 320, a third NFET 338, and a fourth NFET 322.

The CP 350 operates by driving a current across a capacitor 304. A current source or charge pump 302 provides a current to a first node 310. Also, the current source 302 can be either a negative charge source or a positive charge source. A capacitor 304 is coupled to the first node 310 and to ground 308 at a second node 334. The charge leakage is represented by the first leakage current source 306. The first leakage current source 306 is coupled at first end to the first node 310 and at a second end to the second node 334.

In comparison, the correction circuit 352 is more complicated than the CP 350. The correction circuit 352 is coupled to the CP 350 at the first node 310. The drain of the first PFET 312, a first end of the second leakage current source 344, and a first end of the second capacitor are coupled to the first node 310. A second end of the second capacitor 316 and a second end of the second current leakage source 344 are coupled at a third node 332 to the drain of the first NFET 318. Also, the gate of the first NFET 318 is coupled to the body of the first NFET 318 is coupled to the fourth node 330. The body of the second NFET 320 is also coupled to the fourth node 330. Also, the sources of the first NFET 318 and the second NFET 320 are coupled to ground 308.

In addition to the aforementioned connections, there are a variety of other connections that should be made for the current mirror 352 to operate. The drain of the second NFET 320, the source of the third NFET 338, and the source of the fourth NFET 322 are coupled to a fifth node 336. The drain of the third NFET 338, the source of the first PFET 312, and the source of the second PFET 314 are coupled to a voltage source 346. The drain of the fourth NFET 322, the drain of the second PFET 314, and the gate of the second PFET are coupled to a sixth node 328. The gate of the

second PFET 314 is also coupled to the gate of the first PFET 312 through a seventh node 324.

The gates of the third NFET 338 and the fourth NFET 322 are then coupled to the CP 350 (not shown). The voltages input into the gate of the fourth NFET 322 at an eighth node 342 and into the gate of the third NFET 338 at a ninth node 340 vary depending on the state of the current source 302. If the current source is at a high impedance state, as described in FIGURE 1, then an active high signal is input into the gate of the fourth NFET 322 at the eighth node 342. If the current source is not at a high impedance state, as described in FIGURE 1, then an active high signal is input into the gate of the third NFET 338 at a ninth node 340.

The circuit 300 further maintains the voltage on the first capacitor 304 of the CP 350 by using the characteristics of the correction circuit 352. The first capacitor 304 has a first area (A) and a first capacitance (C) associated with it. The second capacitor 316 is a replica of the first capacitor 304 with a second area (A/N) and a second capacitance (C/N), where N is a scaling factor. The width (W) and length (L) of the current mirror 350 is varied such that the voltage across the second capacitor 316 is substantially equal to the voltage across the first capacitor 304. Therefore, since the voltage across the second capacitor 316 is substantially equal to the voltage

across the first capacitor 304 and since the area of the second capacitor 316 is decreased by a factor of N, then the charge leakage represented by the second leakage current source 316 is also decreased by a factor of N (I_{leak}/N).

The reduced current can then be multiplied by N+1 by using N+1 identical mirror devices in parallel. The identical mirrors comprise the second NFET 320, the third NFET 338, the fourth NFET 322, and the second PFET 314. Also, a device with a width ((N+1)W) to develop a tail current equal to a second reduced current ($(N+1)I_{leak}/N$) for a the first PFET 312.

The first PFET 312 is configured such that a first reduced current ($(N+1)I_{leak}/N$) is injected into first node 310 using additional current mirrors to exactly compensate the leakage of the first capacitors 304 and the second capacitor 316 during the hold state. In this manner the effective leakage current is reduced to zero. Additional area required by the circuit is negligible since N can be large and the mirror devices can be small.

It will further be understood from the foregoing description that various modifications and changes may be made in the preferred embodiment of the present invention without departing from its true spirit. This description is intended for purposes of illustration only and should not be construed in a limiting sense. The scope of this invention should be limited only by the language of the following claims.